54SXA Family FPGAs

Specifications

- 8,000 to 72,000 Available Logic Gates
- Up to 360 User-Programmable I/O Pins
- 4,024 Flip-Flops
- 0.25 Micro CMOS

Features

- I/Os with Live, or "Hot," Insertion/Removal Capability
- Power Up/Down Friendly (No Sequencing Required for Supply Voltage)
- 66 MHz PCI
- CPLD and FPGA Integration
- Single Chip Solution
- Configurable I/Os to Support Varity of I/O Standards, Such as 3.3V PCI, LVTTL, TTL, and 5V PCI.
- Configurable Weak Resistor Pullup or Pulldown for Output Tristate at Powerup
- 100% Resource Utilization with 100% Pin Locking
- 2.5V, 3.3V, and 5.0V Mixed Voltage Operation with 5.0V Input Tolerance
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug capability with Silicon Explorer
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, IST, Mentor Graphics, Model Tech, Synopsys, Synplicity, and Viewlogic Design Entry and Simulation Tools
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

SX Product Profile

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Gate Capacity	8,000	16,000	32,000	72,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Register Cells (Dedicated Flip-Flops)	256	528	1,080	2,012
Maximum Flip-Flops	512	990	1,980	4,024
User I/Os (Maximum)	130	177	249	360
Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
JTAG	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes
Clock-to-Out	TBD	TBD	4.5 ns	4.8 ns
Input Set-Up (External)	TBD	TBD	-1.3 ns	-3.3 ns
Speed Grades	Std, –1, –2, –3	Std, –1, –2, –3	Std, –1, –2, –3	Std, –1, –2, –3
Temperature Grades	C, I, M	C, I, M	C, I, M	C, I, M
Packages (by pin count)				
PQFP	208	208	208	208
TQFP	100, 144	100, 144	144	—
PBGA	144	144	144, 256, 329	484

General Description

The New SXA Family of FPGAs

Actel's SXA Family of FPGAs features a revolutionary new sea-of-modules architecture that delivers next-generation device performance and integration levels not currently achieved by any other FPGA architecture. SXA devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further speed time-to-market for performance-intensive applications.

Fast and Flexible New Architecture

Actel's SXA architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. Optimal use of the silicon is made by locating the routing and interconnect resources in the metal layers above the logic modules. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules.

To minimize signal propagation delay, SXA devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (typically 90% of connections use only three antifuses). The unique local and general routing structure featured in SXA devices gives fast and predictable performance, allows 100% pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with a minimum of effort.

Further complementing the SXA's flexible routing structure is a hard-wired, constantly-loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SXA devices have easy-to-use I/O cells which do not require HDL instantiation, facilitating design re-use and reducing design and debugging time.

Ordering Information

A54SX16 A – 2 PQ 208

Application (Temperature Range)
- Blank = Commercial (0 to +70 C)
- I = Industrial (–40 to +85 C)
- M = Military (–55 to +125 C)
- PP = Pre-production

Package Lead Count

Package Type
- BG = 1.27mm Ball Grid Array
- fBG = 1.0 mm Ball Grid Array
- PQ = Plastic Quad Flat Pack
- TQ = Thin (1.4 mm) Quad Flat Pack

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% Faster than Standard
- –2 = Approximately 25% Faster than Standard
- –3 = Approximately 35% Faster than Standard

A = 0.25 Micro CMOS Technology

Part Number
- A54SX08A = 8,000 Gates
- A54SX16A = 16,000 Gates
- A54SX32A = 32,000 Gates
- A54SX72A = 72,000 Gates

Product Plan

	Speed Grade*				Application		
	Std	–1	–2	–3	C	I†	M•
A54SX08A Device							
100-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
144-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	P	P
144-Pin Plastic Ball Grid Array (fBGA)	P	P	P	P	P	P	P
A54SX16A Device							
100-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
144-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	P	P
144-Pin Plastic Ball Grid Array (fBGA)	P	P	P	P	P	P	P
256-Pin Plastic Ball Grid Array (fBGA)	P	P	P	P	P	P	P
A54SX32A Device							
144-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	P	✔	✔	P
144-Pin Plastic Ball Grid Array (fBGA)	P	P	P	P	P	P	P
256-Pin Plastic Ball Grid Array (fBGA)	P	P	P	P	P	P	P
329-Pin Plastic Ball Grid Array (BGA)	✔	✔	✔	P	✔	✔	P
A54SX72A Device							
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	P	✔	✔	P
484-Pin Plastic Ball Grid Array (fBGA)	✔	✔	✔	P	✔	✔	P

Consult your local Actel sales representative for product availability.

Applications: *C = Commercial*, *I = Industrial*, *M = Military*

Availability: ✔ = *Available*, *P = Planned*, — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% Faster than Standard*, *–2 = Approx. 25% Faster than Standard*, *–3 = Approx. 35% Faster than Standard*

† Only Std, –1, –2 Speed Grade

• Only Std, –1 Speed Grade

Plastic Device Resources

Device	User I/Os (including clock buffers)						
	PQFP 208-Pin	TQFP 100-Pin	TQFP 144-Pin	fBGA 144-Pin	fBGA 256-Pin	BGA 329-Pin	fBGA 484-Pin
A54SX08A	130	81	113	TBD	—	—	—
A54SX16A	175	81	113	TBD	—	—	—
A54SX32A	174	—	113	TBD	TBD	249	—
A54SX72A	173	—	—	—	—	—	360

Package Definitions *(Consult your local Actel sales representative for product availability.)*

PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, BGA = 1.27mm Plastic Ball Grid Array, fBGA = 1.0mm Plastic Ball Grid Array.

Pin Description

CLKA/B Clock A and B

TTL/3.3V PCI clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

QCLKA/B/C/D Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs. They are TTL/3.3V PCI clock input for clock distribution networks. Each of these clock inputs can drive up to a quarter of the chip, and they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (These quadrant clocks are only for 54SX72A).

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode (refer to the JTAG pins functionality table), TCK becomes active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tri-stated by the Designer Series software.

TMS Test Mode Select

The TMS pin controls the use of JTAG pins (TCK, TDI, TDO). In flexible mode (refer to the JTAG pins functionality table), when the TMS pin is set LOW, the TCK, TDI, and TDO pins are JTAG pins. Once the JTAG pins are in JTAG mode they will remain in JTAG mode until the internal JTAG state machine reaches the "logic reset" state. At this point the JTAG pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated JTAG mode, TMS functions as specified in the IEEE 499.1 JTAG Specifications. JTAG operation is further described on page 10.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed.

PRB Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed.

TDI Test Data Input

Serial input for JTAG and diagnostic probe. In flexible mode, (refer to the JTAG pins functionality table), TDI is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for JTAG. In flexible mode (Refer to the JTAG pins functionality table), TDO is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

V_{CCI} Supply Voltage

Supply voltage for I/Os.

V_{CCA} Supply Voltage

Supply voltage for Array.

Table 1 • *Supply Voltages*

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
A54SX08A A54SX16A A54SX32A A54SX72A	2.5V	2.5V	5.0V	2.5V
	2.5V	3.3V	5.0V	3.3V
	2.5V	5.0V	5.0V	5.0V

SXA Family Architecture

The SXA Family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

Actel's new SXA Family provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SXA Family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

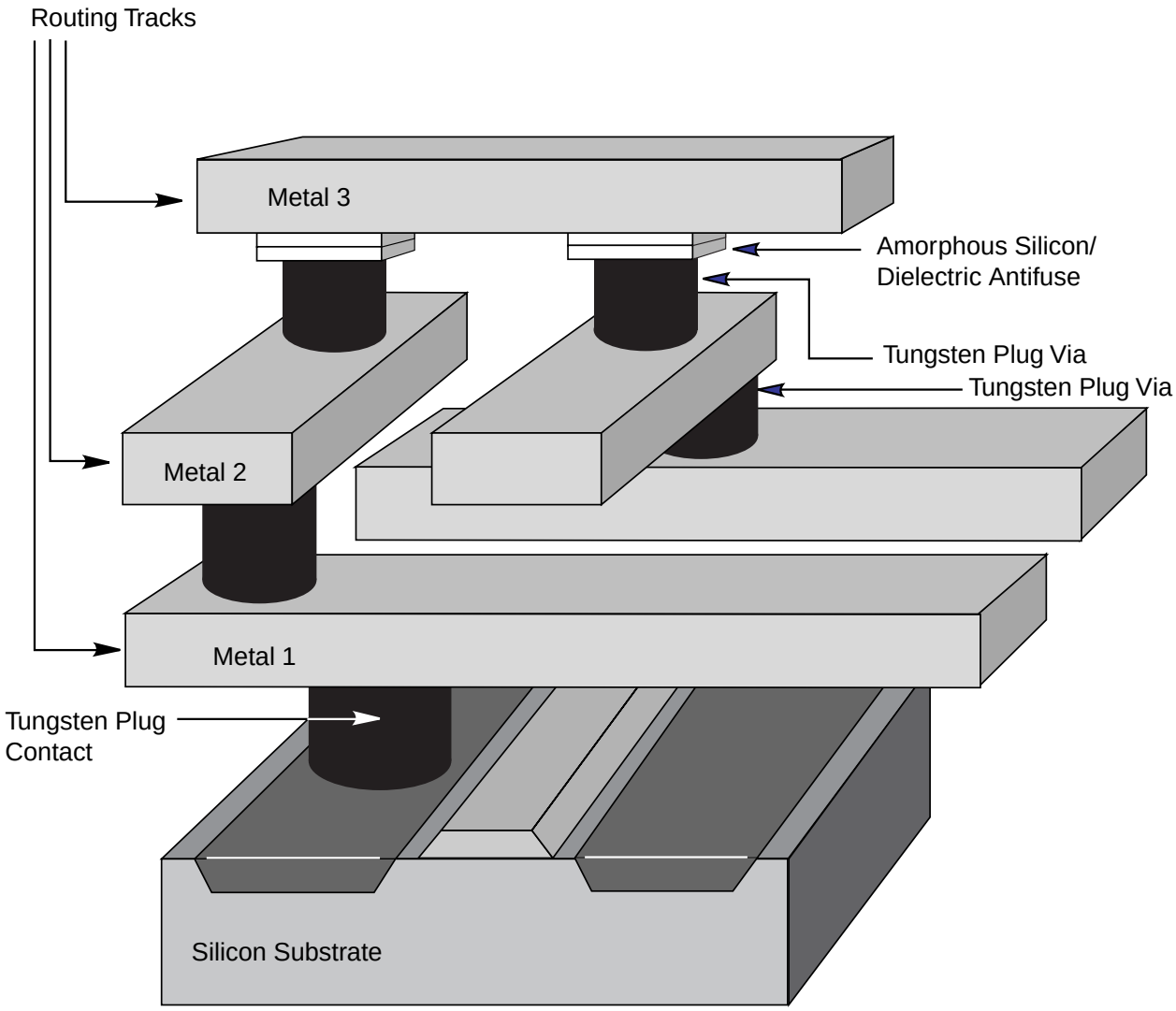


Figure 1 • *SXA Family Interconnect Elements*

Logic Module Design

The SXA Family architecture has been called a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing (see Figure 2). Actel provides two types of logic modules, the R-cell and the C-cell.

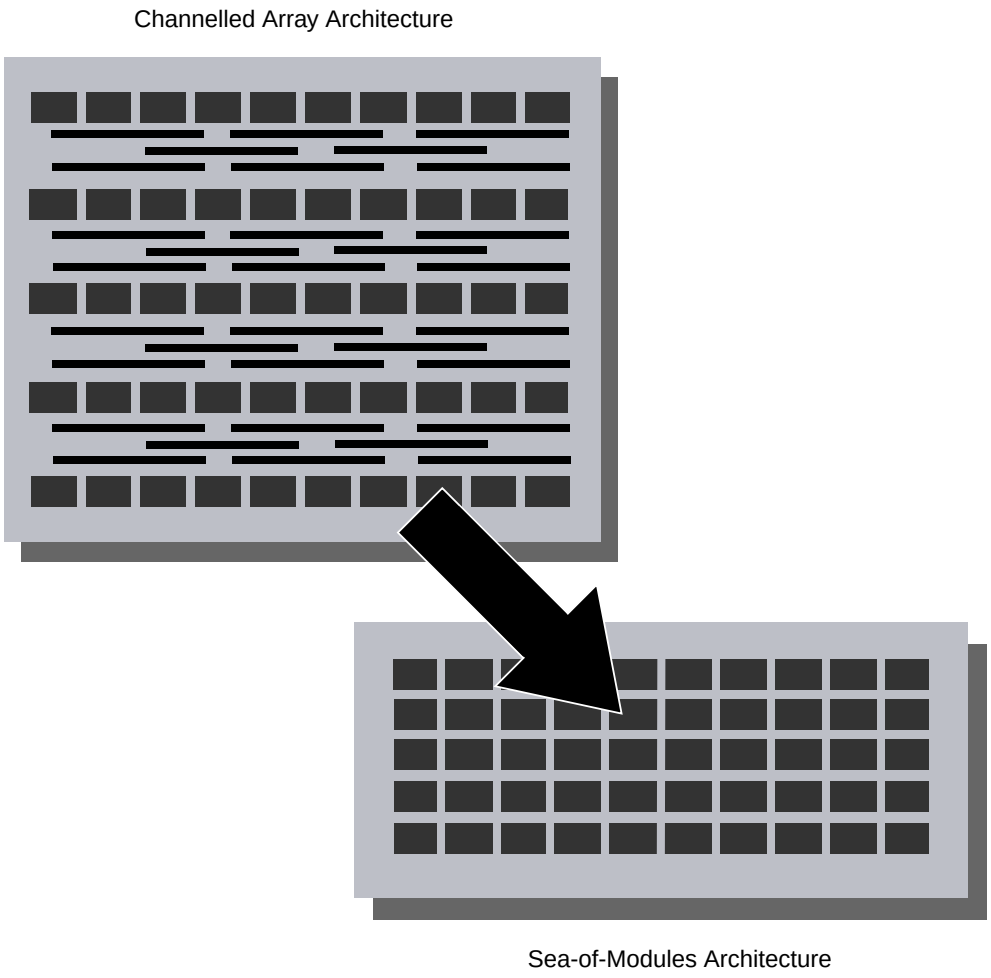


Figure 2 • *Channelled Array and Sea-of-Modules Architectures*

The R-cell (or register cell) contains a flip-flop featuring more control signals than in previous Actel architectures, including asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines). The R-cell (Figure 3) registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while allowing mapping of synthesized functions into the SXA FPGA. The clock source for the R-cell can be chosen from the hard-wired clock or the routed clock.

The C-cell (or combinatorial cell, Figure 4) implements a range of combinatorial functions up to 5-inputs. Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SXA architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SXA Family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

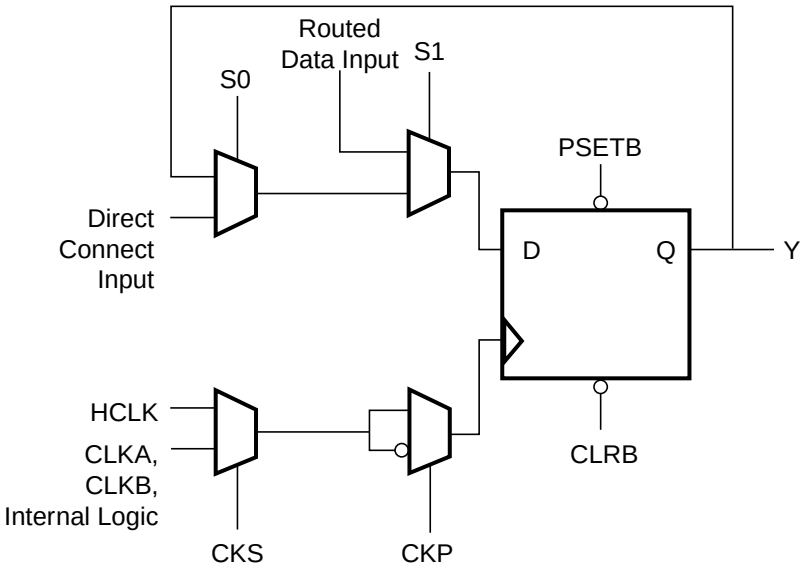


Figure 3 • *R-Cell*

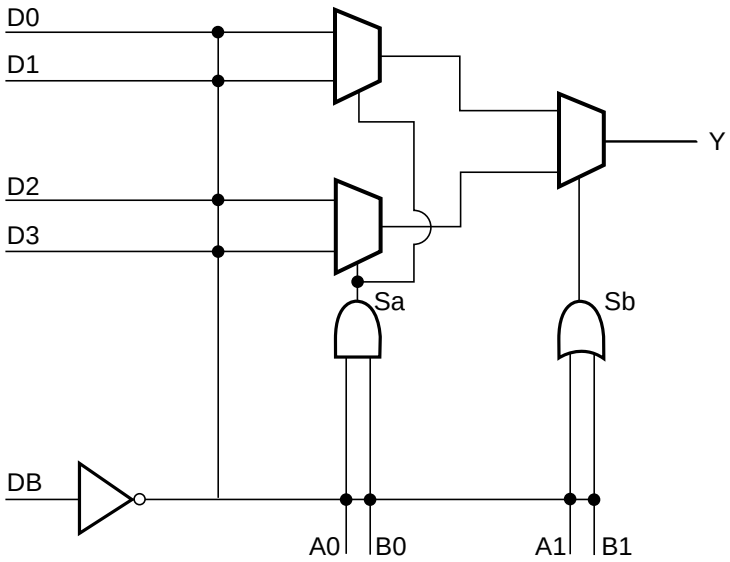


Figure 4 • *C-Cell*

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 5). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SXA devices feature significantly more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 6 and Figure 7). This routing architecture also dramatically reduces the

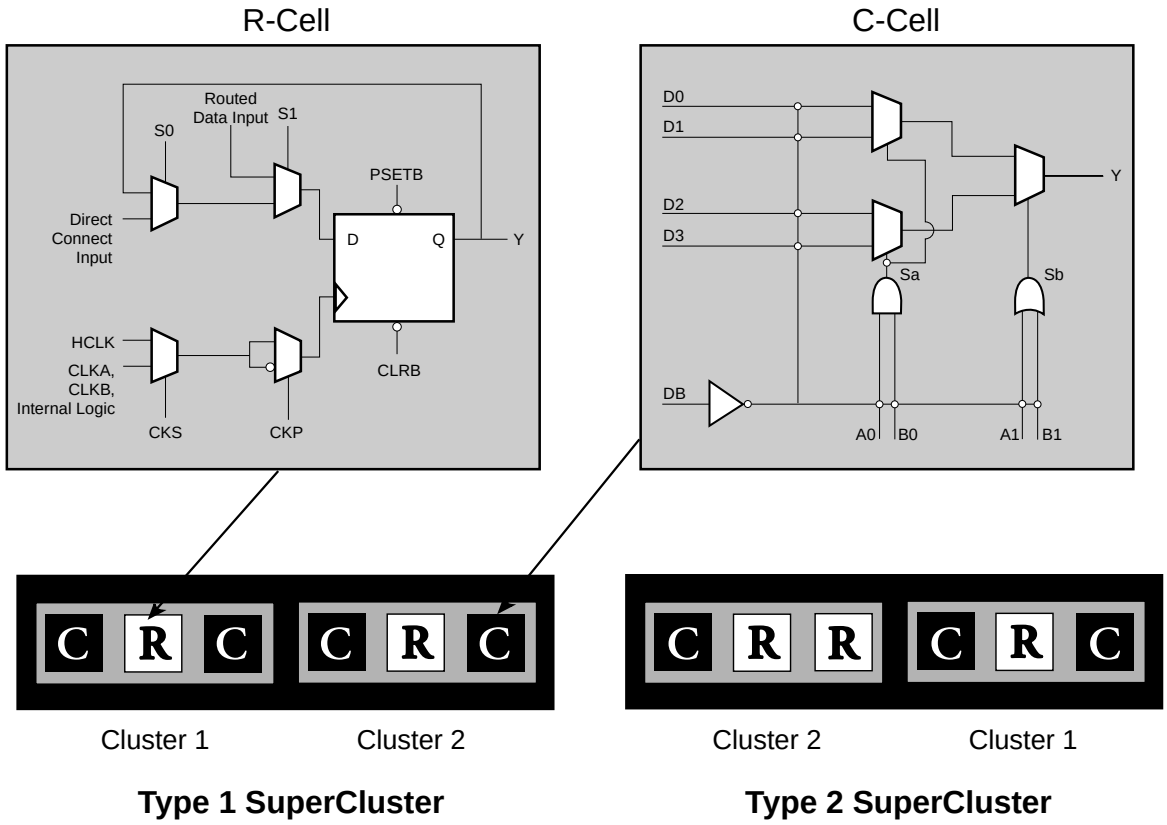


Figure 5 • *Cluster Organization*

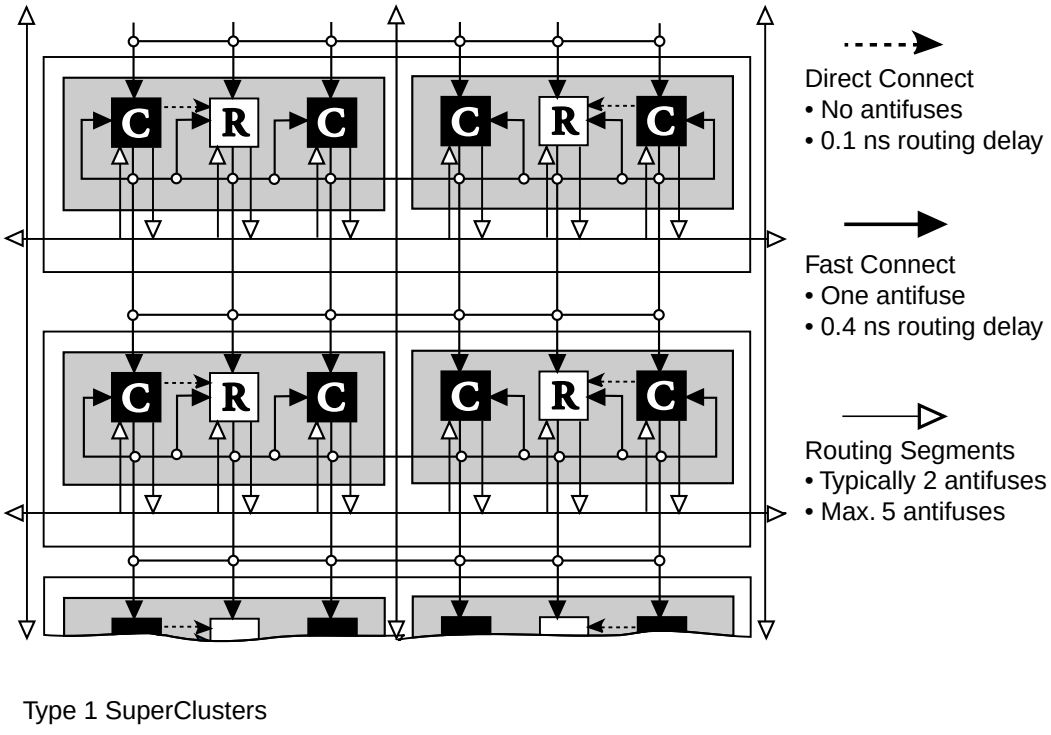


Figure 6 • *DirectConnect and FastConnect for Type 1 SuperClusters*

number of antifuses required to complete a circuit, ensuring the highest possible performance.

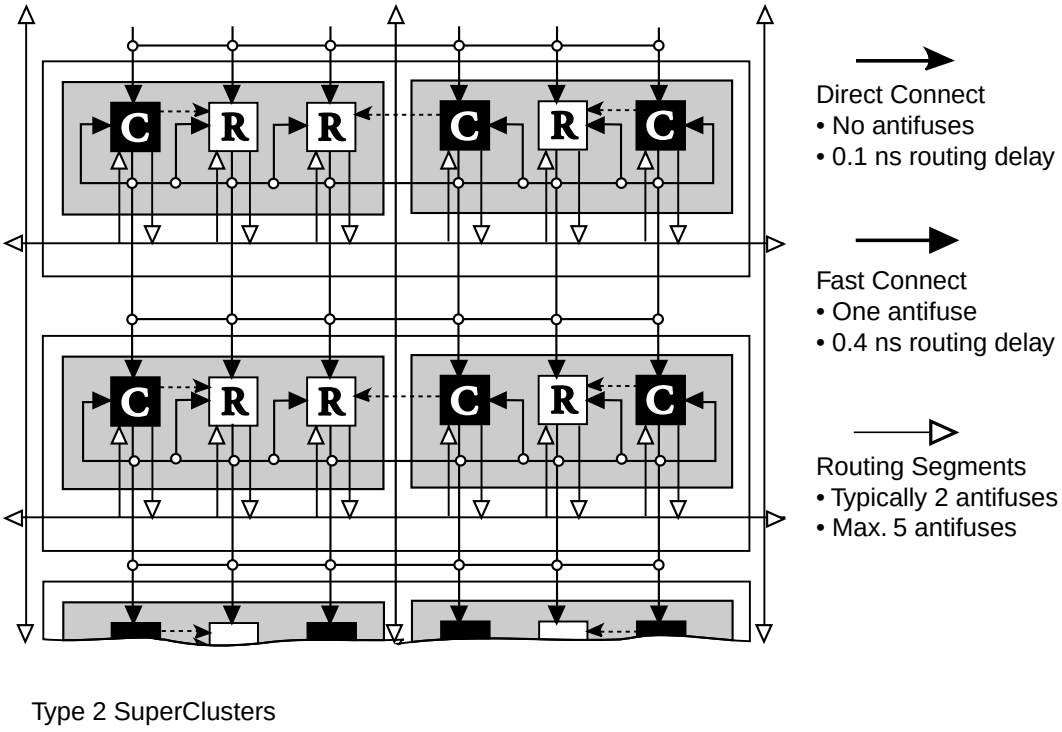


Figure 7 • *DirectConnect and FastConnect for Type 2 SuperClusters*

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.2 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place and route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard-wired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal, enabling the 4.0 ns clock-to-out (pin-to-pin) performance of the SXA devices. The hard-wired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal signal logic within the SXA device.

Other Architecture Features

Technology

Actel's SXA Family of FPGAs is implemented in high-voltage twin-well CMOS using three layers of metal and 0.25 micron design rules (moving quickly to 0.22 micron). The M2/M3 antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals, and has a programmed ("on" state) resistance of 25 ohms with capacitance of 1.6 fF for low signal impedance.

Performance

The combination of architectural features described above enables SXA devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the Actel SXA Family is an optimal platform upon which to integrate the functionality previously contained in multiple

CPLDs. In addition, designs which previously would have required a gate array to meet performance goals can now be integrated into an SXA device with dramatic improvements in cost and time-to-market. Using timing-driven place and route tools, designers can achieve highly deterministic device performance.

With SXA devices, designers can achieve a higher level of performance without recourse to complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code.

I/O Modules

Each I/O on an SXA device can be configured as an input, an output, a tri-state output, or a bi-directional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 4.0 ns, and external set-up time as low as 0.6 ns. I/O cells including embedded latches and flip-flops require instantiation in HDL code, a complication not required by SXA FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reducing overall design time.

Power Requirements

The SXA Family supports 3.3-volt operation and is designed to tolerate 5-volt inputs. Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as an SRAM or EPROM does), thereby making it the lowest-power architecture on the market.

JTAG

All SXA devices are IEEE 1149.1 (JTAG) compliant. SXA devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse. The functionality of each pin is described in Table 2.

Table 2 • *JTAG*

Program Fuse Blown (Dedicated JTAG Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10K ohm on TMS

In the dedicated JTAG mode, TCK, TDI and TDO are dedicated JTAG pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10K ohm. TMS can be pulled LOW to initiate the JTAG sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Design Tool Support

As with all Actel FPGAs, the new SXA Family is fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.

Silicon Explorer and SXA FPGA

Actel SXA FPGAs include internal Probe circuitry to dynamically observe and analyze any signal inside the FPGA during normal device operation. The Probe circuitry is accessed and controlled by Silicon Explorer--an integrated debugging and logic analysis tool that attaches to a PC. Silicon Explorer is also an 18-channel logic analyzer that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Two channels of the logic analyzer have a direct connection to PRA and PRB pins, which can automatically display any two signals inside the FPGA. The remaining 16 channels of the logic analyzer can be used to examine other signals on the board. In addition, Silicon Explorer can read back the design's checksum, allowing designers to verify that the correct design was programmed in the FPGA.

SXA Probe Circuit Control Pins

The Silicon Explorer tool uses the JTAG ports (TDI, TCK, TMS and TDO) to select the desired nets for debugging. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 8 illustrates the interconnection between Silicon Explorer and the FPGA to perform in-circuit debugging.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA and PRB pins as input or bi-directional ports. Because these pins are active during probing, critical signal input through these pins is not available while probing. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuitry.

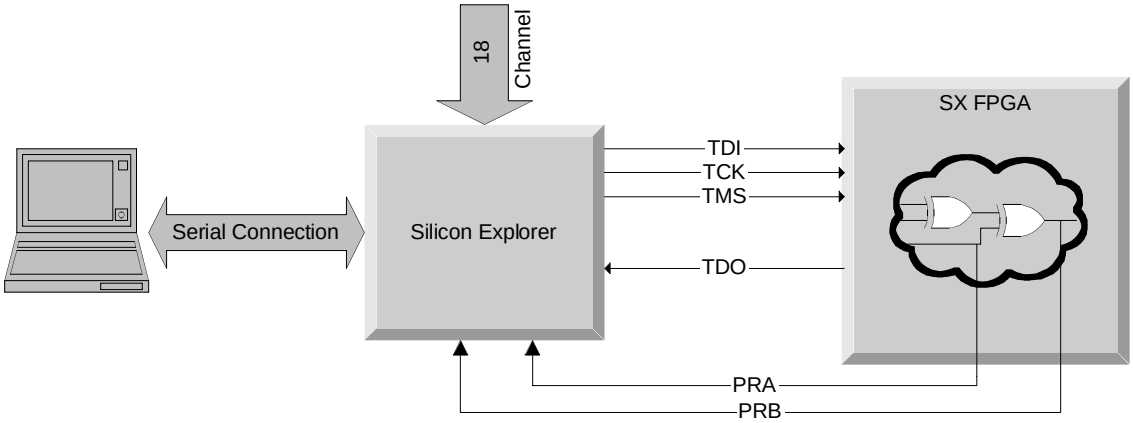


Figure 8 • *Probe Setup*

3.3V/5V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage[2]	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +2.7	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
3.3V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS)	(V_{CCI} – 0.1)	V_{CCI}	(V_{CCI} – 0.1)	V_{CCI}	V
	(I_{OH} = -8mA) (TTL)	2.4	V_{CCI}			
	(I_{OH} = -6mA) (TTL)			2.4	V_{CCI}	
V_{OL}	(I_{OL}= 20uA) (CMOS)		0.10			V
	(I_{OL} = 12mA) (TTL)		0.50			
	(I_{OL} = 8mA) (TTL)				0.50	
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See “Evaluating Power in 54SXA Devices” on page 20.				

PCI Compliance for the 54SXA Family

The 54SXA family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5.0V PCI Operation)

Table 3 • *DC specifications for 5V Signaling*

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for IOs		4.75	5.25	V
V_{IH}	Input High Voltage[1]		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	A
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	A
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, FRAME#, IRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

AC Specifications (5.0V PCI Operation)

Table 4 • *AC Specifications for 5V Signaling*

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching[1] Current High[1, 2] [1, 3] (Test Point)[3]	$0 < V_{OUT} \le 1.4$ $1.4 \le V_{OUT} < 2.4$ $3.1 < V_{OUT} < V_{CC}$ $V_{OUT} = 3.1$	–44 $-44 + (V_{OUT} - 1.4)/0.024$	 Eq. A –142	mA mA mA
$I_{OL(AC)}$	Switching[1] Current High[1] [1, 3] (Test Point)[3]	$V_{OUT} \ge 2.2$ $2.2 > V_{OUT} > 0.55$ $0.71 > V_{OUT} > 0$ $V_{OUT} = 0.71$	95 $V_{OUT}/0.023$	 Eq. B 206	mA mA mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[4]	0.4V to 2.4V load	1	5	V/ns
$slew_F$	Output Fall Slew Rate[4]	2.4V to 0.4V load	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 9. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 9. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

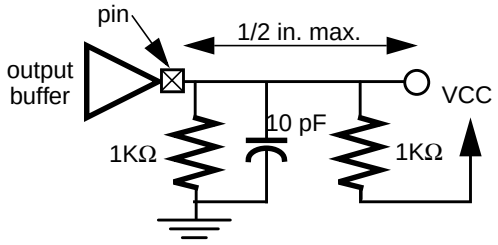


Figure 9 shows the 5.0V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P family.

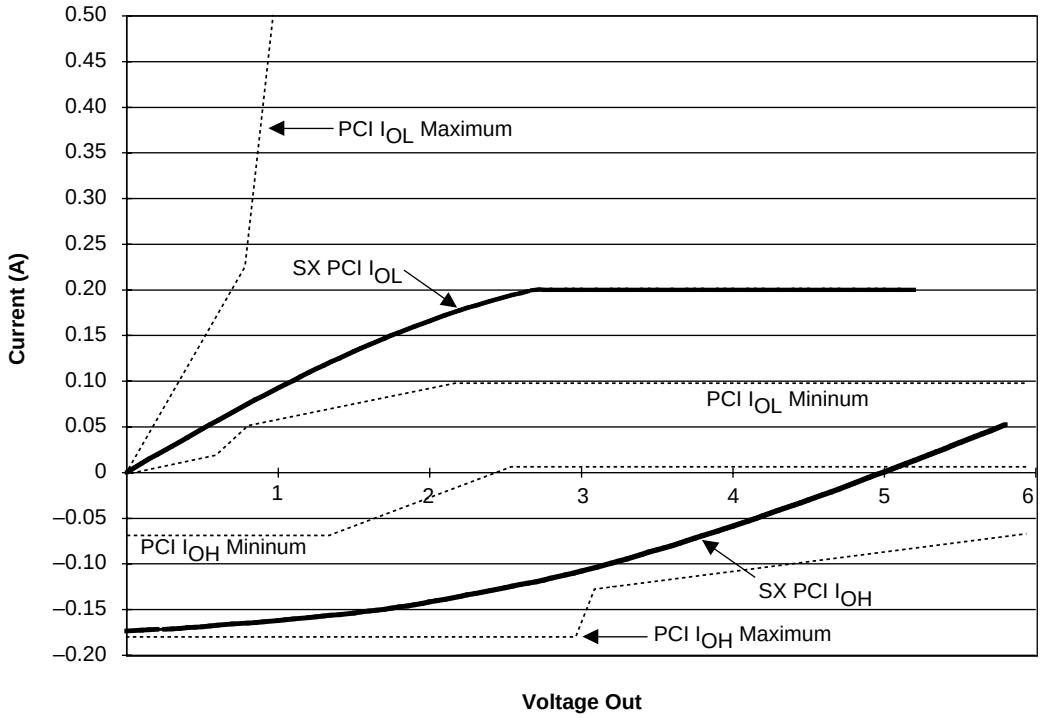


Figure 9 • *5.0V PCI Curve for SXA Family*

Equation A:

$$I_{OH} = 11.9 * (V_{OUT} – 5.25) * (V_{OUT} + 2.45)$$

for $V_{CC} > V_{OUT} > 3.1V$

Equation B:

$$I_{OL} = 78.5 * V_{OUT} * (4.4 – V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

DC Specifications (3.3V PCI Operation)

Table 5 • *DC specifications for 3.3V Signaling*

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for IOs		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CC}$		10	A
V_{OH}	Output High Voltage	I_{OUT} = –500 A	$0.9V_{CC}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 A		$0.1V_{CC}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean in general that components for expansion boards would need to use alternatives to ceramic PGA packaging. This would mean in general that components for expansion boards would need to use alternatives to ceramic packaging; i.e., PQFP, SGA, etc.*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

AC Specifications (3.3V PCI Operation)

Table 6 • *AC Specifications for 3.3V Signaling*

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching[1] Current High[1] [1, 2] (Test Point)[2]	$0 < V_{OUT} \le 0.3V_{CC}$ $0.3V_{CC} \le V_{OUT} < 0.9V_{CC}$ $0.7V_{CC} < V_{OUT} < V_{CC}$ $V_{OUT} = 0.7V_{CC}$	$-12V_{CC}$ $-17.1 + (V_{CC} - V_{OUT})$	 Eq. C $-32V_{CC}$	mA mA mA
$I_{OL(AC)}$	Switching[1] Current High[1] [1, 2] (Test Point)[2]	$V_{CC} > V_{OUT} \ge 0.6V_{CC}$ $0.6V_{CC} > V_{OUT} > 0.1V_{CC}$ $0.18V_{CC} > V_{OUT} > 0$ $V_{OUT} = 0.18V_{CC}$	$16V_{CC}$ $26.7V_{OUT}$	 Eq. D $38V_{CC}$	mA mA mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \le -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[3]	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$slew_F$	Output Fall Slew Rate[3]	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 10. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 10. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

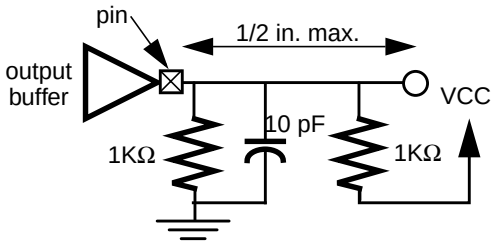


Figure 10 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SXA family.

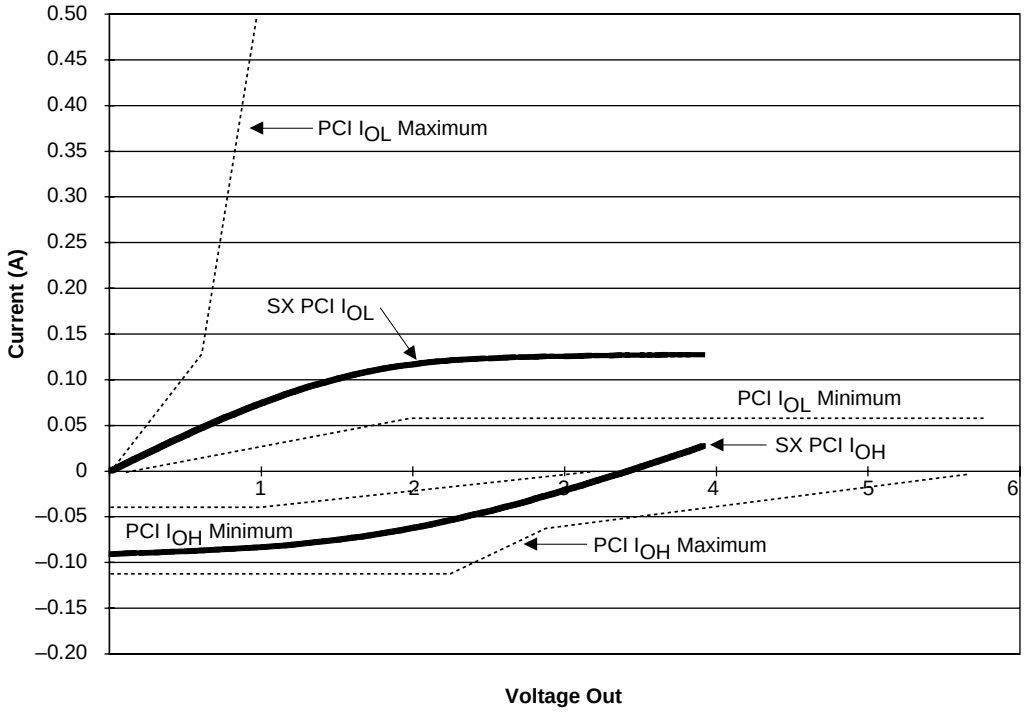


Figure 10 • *3.3V PCI Curve for SXA Family*

Equation C:

$$I_{OH} = (98.0/V_{CC}) * (V_{OUT} - V_{CC}) * (V_{OUT} + 0.4V_{CC})$$

for $V_{CC} > V_{OUT} > 0.7\ V_{CC}$

Equation D:

$$I_{OL} = (256/V_{CC}) * V_{OUT} * (V_{CC} - V_{OUT})$$

for $0V < V_{OUT} < 0.18\ V_{CC}$

Power-Up Sequencing

V_{CCA}	V_{CCI}	Power-Up Sequence	Comments
A54SX08A, A54SX16A, A54SX32A, A54SX72A			
2.5V	2.5V	V_{CCA} First V_{CCI} Second	No possible damage to device.
		V_{CCI} First V_{CCA} Second	No possible damage to device.
2.5V	3.3V	2.5V First 3.3V Second	No possible damage to device.
		3.3V First 2.5V Second	No Possible damage to device.
2.5V	5.0V	2.5V First 5.0V Second	No possible damage to device.
		5.0V First 2.5V Second	No possible damage to device.

Power-Down Sequencing

V_{CCA}	V_{CCI}	Power-Down Sequence	Comments
A54SX08A, A54SX16A, A54SX32A, A54SX72A			
2.5V	2.5V	V_{CCA} First V_{CCI} Second	No possible damage to device.
		V_{CCI} First V_{CCA} Second	No possible damage to device.
2.5V	3.3V	2.5V First 3.3V Second	No Possible damage to device.
		3.3V First 2.5V Second	No possible damage to device.
2.5V	5.0V	2.5V First 5.0V Second	No possible damage to device.
		5.0V First 2.5V Second	No possible damage to device.

Junction Temperature (T_J)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use Equation 4, shown below, to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (4)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Package Thermal Characteristics section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 144-pin package at commercial temperature and still air is as follows:

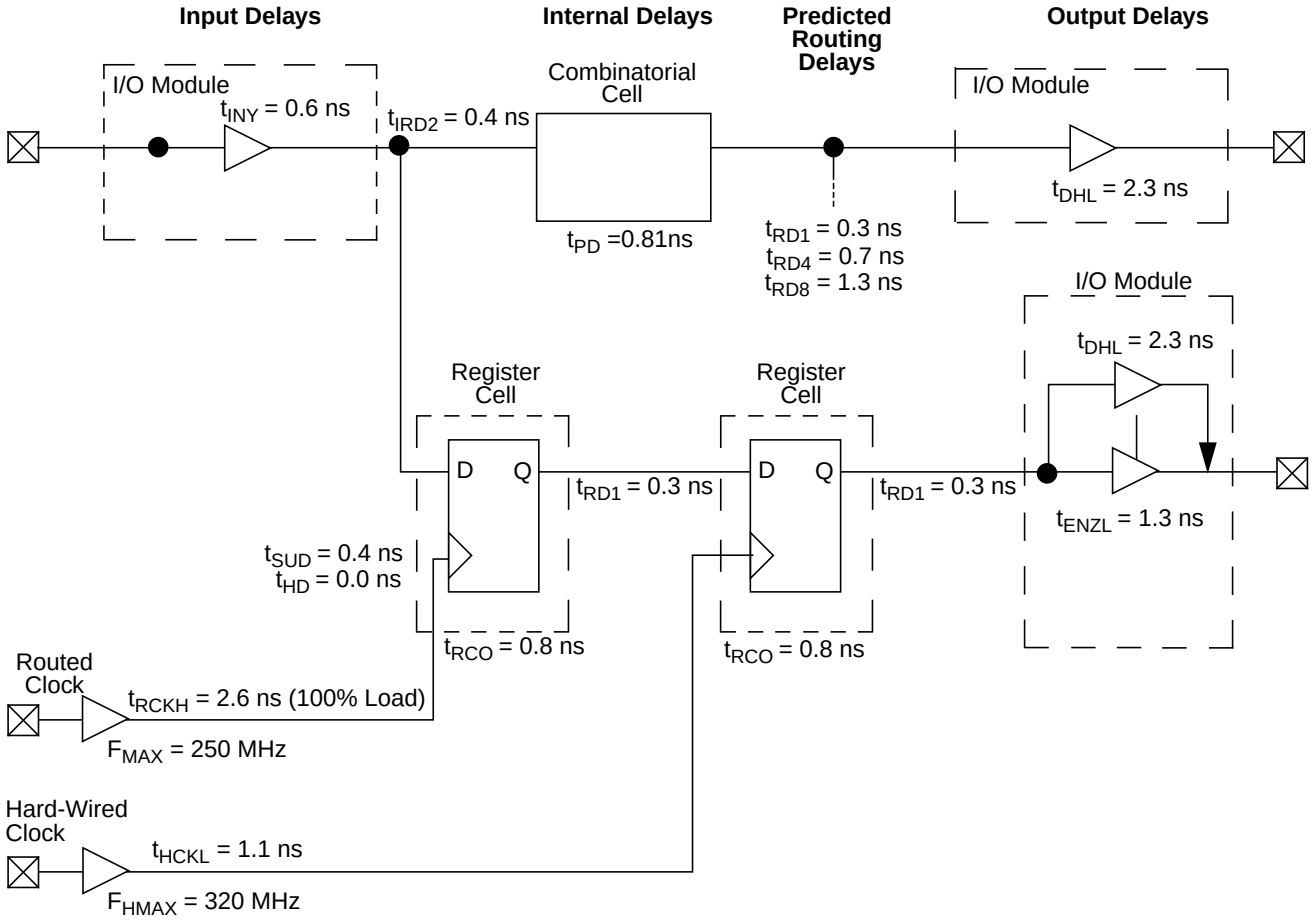
$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{jA}\ (°C/W)} = \frac{150°C - 70°C}{32\ °C/W} = 2.5W$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Thin Quad Flatpack (TQFP)	100	12	37.5	30	°C/W
Thin Quad Flatpack (TQFP)	144	10	32	24	°C/W
Plastic Quad Flatpack (PQFP) with Heat Spreader	208	8	18	14	°C/W
Plastic Ball Grid Array (fBGA)	144	3.8	38.8	26.7	°C/W
Plastic Ball Grid Array (fBGA)	256	3.3	30	25	°C/W
Plastic Ball Grid Array (BGA)	329	3	18	13.5	°C/W
Plastic Ball Grid Array (fBGA)	484	0.8	20	15	°C/W

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.7V)

V_{CCA}	Junction Temperature (T_J)						
	–55	–40	0	25	70	85	125
2.3	0.80	0.85	0.94	0.95	1.07	1.11	1.24
2.5	0.75	0.79	0.88	0.89	1.00	1.04	1.16
2.7	0.71	0.74	0.83	0.84	0.94	0.98	1.09

54SXA Timing Model*



**Values shown for A54SX32A-3, worst-case commercial conditions.*

Hard-Wired Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKL}$
= 0.6 + 0.3 + 0.4 – 1.1 = 0.2 ns

Clock-to-Out (Pin-to-Pin)
= $t_{HCKL} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.1 + 0.8 + 0.3 + 2.3 = 4.5 ns

Routed Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 0.6 + 0.3 + 0.4 – 2.6 = -1.3 ns

Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 2.6 + 0.8 + 0.3 + 2.3 = 6.0 ns

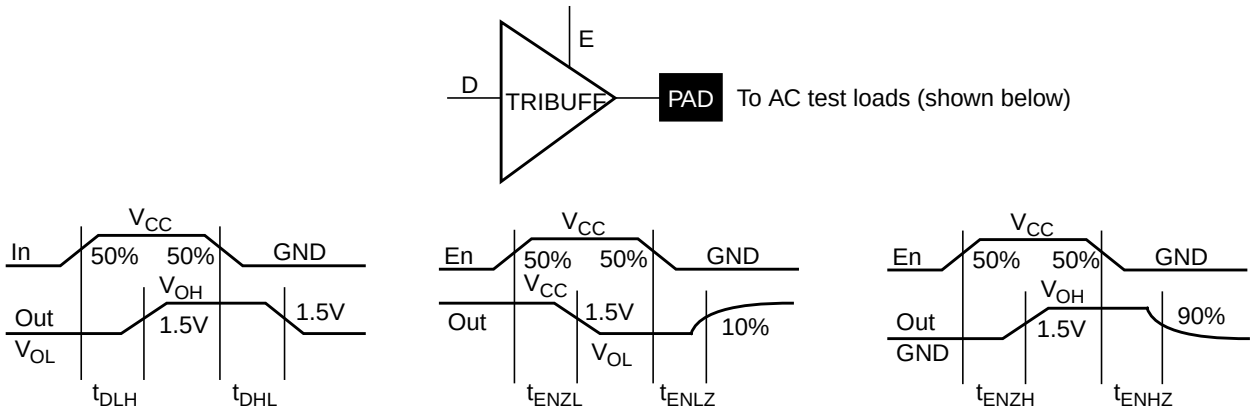
Timing Characteristics

Timing characteristics for 54SXA devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all 54SXA family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

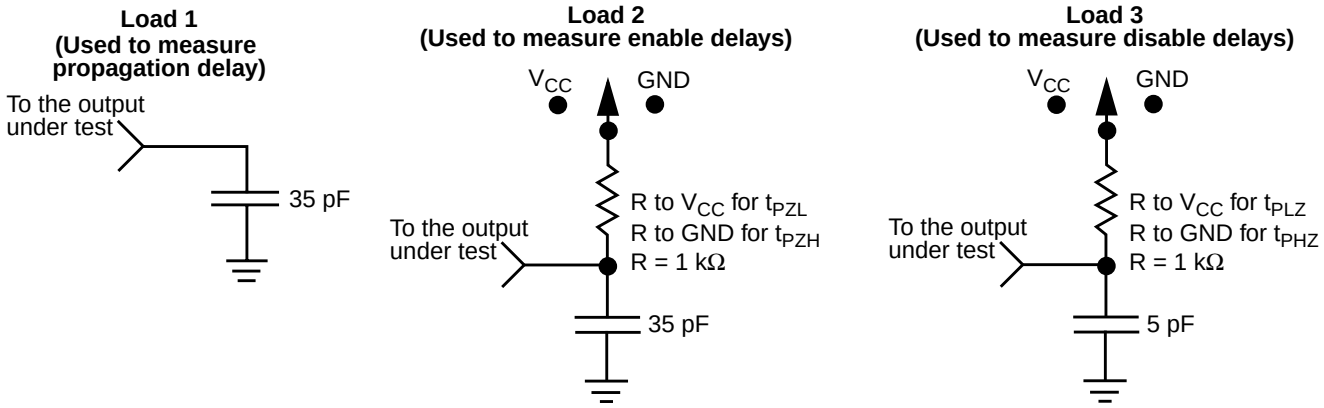
Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

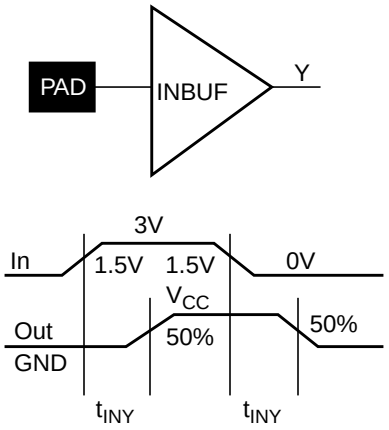
Output Buffer Delays



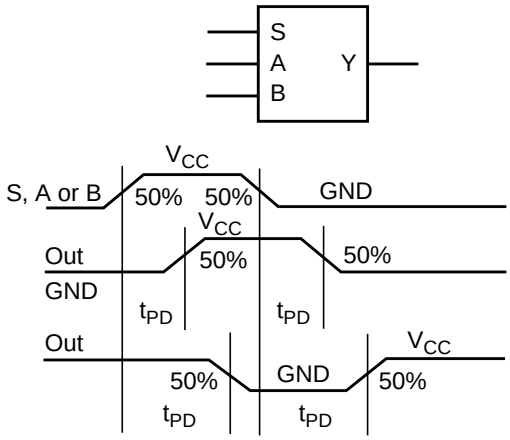
AC Test Loads



Input Buffer Delays

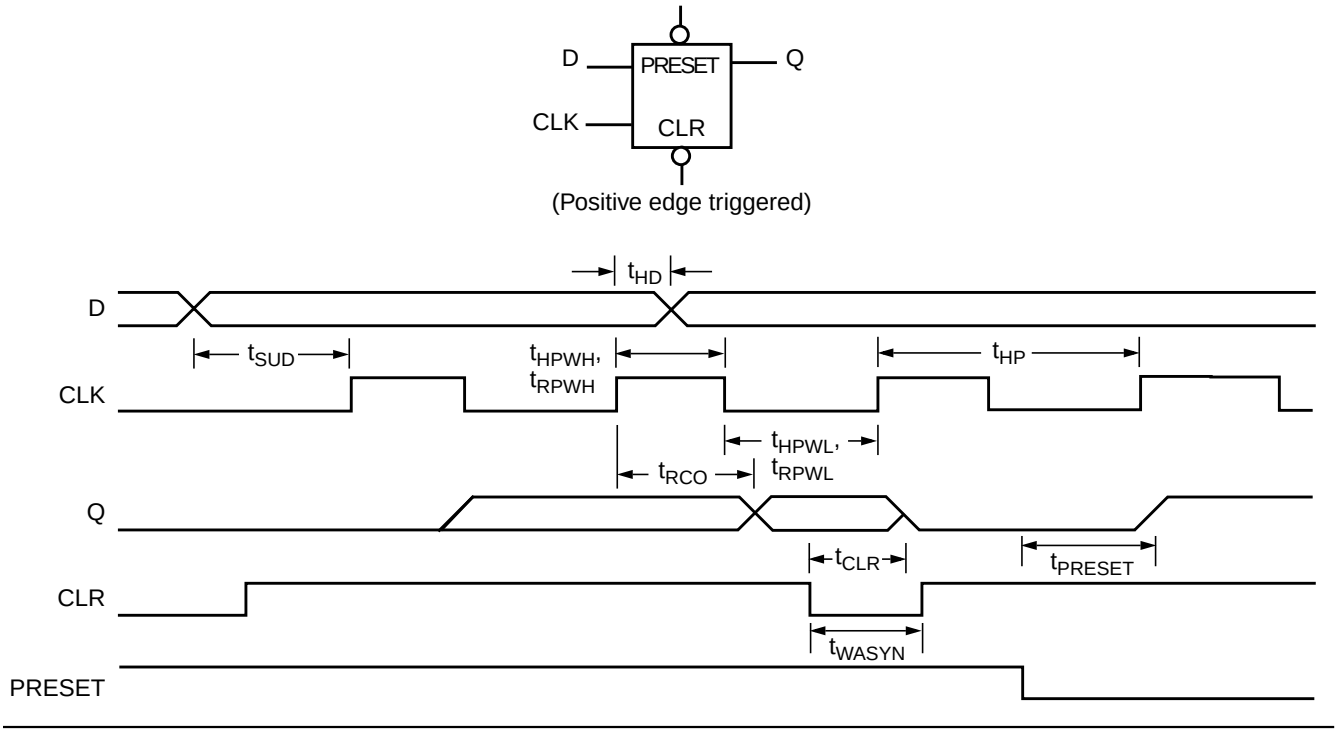


C-Cell Delays



Register Cell Timing Characteristics

Flip-Flops



Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the data sheet specifications section.

Timing Derating

54SXA devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

C-Cell Propagation Delays[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		0.8		0.9		1.1		1.3	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.1		0.2		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7	ns
t_{RD3}	FO=3 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1	ns
t_{RD8}	FO=8 Routing Delay		1.3		1.5		1.7		2.1	ns
t_{RD12}	FO=12 Routing Delay		1.9		2.2		2.5		3.0	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		0.9		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.8		0.9	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.4		0.5		0.6		0.7		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.0		1.2		1.4		1.6		ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.7		0.8		0.9	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.0		1.2		1.4	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7	ns
t_{IRD3}	FO=3 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1	ns
t_{IRD8}	FO=8 Routing Delay		1.3		1.5		1.7		2.1	ns
t_{IRD12}	FO=12 Routing Delay		1.9		2.2		2.5		3.0	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32A Timing Charateristics (continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70 C)

I/O Module – PCI Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.4		2.8		3.2		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.3		2.7		3.1		3.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.6		1.9		2.1		2.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.6		2.9		3.3		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.8		4.4	ns

Note:

1. Delays based on 10pF loading.

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70 C)

I/O Module – TTL Output Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.7		4.2		4.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3		3.7		4.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		3.0		3.4		4.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.2		3.7		4.2		4.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.2		3.6		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.3		3.8		4.3		5.0	ns

A54SX32A Timing Charateristics (continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3 V, V_{CCI} = 4.75 V, T_J = 70 C)

I/O Module – TTL Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.5		2.9		3.3		3.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.1		3.6		4.1		4.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		3.0		3.4		4.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.4		3.9		4.4		5.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.2		4.8		5.5		6.313	ns

(Worst-Case Commercial Conditions V_{CCA} = 3.0 V, V_{CCI} = 4.75 V, T_J = 70 C)

I/O Module – PCI Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.2		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.4		3.9		4.5		5.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.6		3.0		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.3		3.9		4.4		5.2	ns

A54SX32A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.4		1.6		1.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.4		1.7	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.1		0.2		0.2		0.2	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.8		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.0		2.3		2.6		3.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.0		2.4		2.7		3.1	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.2		2.5		2.8		3.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.6		3.0		3.4		4.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.6		3.0		3.4		4.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0	ns

A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA},V_{CCI} = 3.0V, T_J = 70°C)

C-Cell Propagation Delays[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		0.8		0.9		1.1		1.3	ns
Predicted Routing Delays[2]										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.1		0.2		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7	ns
t_{RD3}	FO=3 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1	ns
t_{RD8}	FO=8 Routing Delay		1.3		1.5		1.7		2.1	ns
t_{RD12}	FO=12 Routing Delay		1.9		2.2		2.5		3.0	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		0.9		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.8		0.9	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.4		0.5		0.6		0.7		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.0		1.2		1.4		1.6		ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX72A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.7		0.8		0.9	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.0		1.2		1.4	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7	ns
t_{IRD3}	FO=3 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1	ns
t_{IRD8}	FO=8 Routing Delay		1.3		1.5		1.7		2.1	ns
t_{IRD12}	FO=12 Routing Delay		1.9		2.2		2.5		3.0	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX72A Timing Charateristics (continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70 C)

I/O Module – PCI Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.4		2.8		3.2		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.3		2.7		3.1		3.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.6		1.9		2.1		2.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.6		2.9		3.3		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.8		4.4	ns

Note:

1. Delays based on 10pF loading.

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70 C)

I/O Module – TTL Output Timing		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.7		4.2		4.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3		3.7		4.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		3.0		3.4		4.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.2		3.7		4.2		4.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.2		3.6		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.3		3.8		4.3		5.0	ns

A54SX72A Timing Charateristics (continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3 V, V_{CCI} = 4.75 V, T_J = 70 C)

I/O Module – TTL Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.5		2.9		3.3		3.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.1		3.6		4.1		4.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		3.0		3.4		4.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.4		3.9		4.4		5.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.2		4.8		5.5		6.3	ns

(Worst-Case Commercial Conditions V_{CCA} = 3.0 V, V_{CCI} = 4.75 V, T_J = 70 C)

I/O Module – PCI Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.2		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.4		3.9		4.5		5.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.6		3.0		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.3		3.9		4.4		5.2	ns

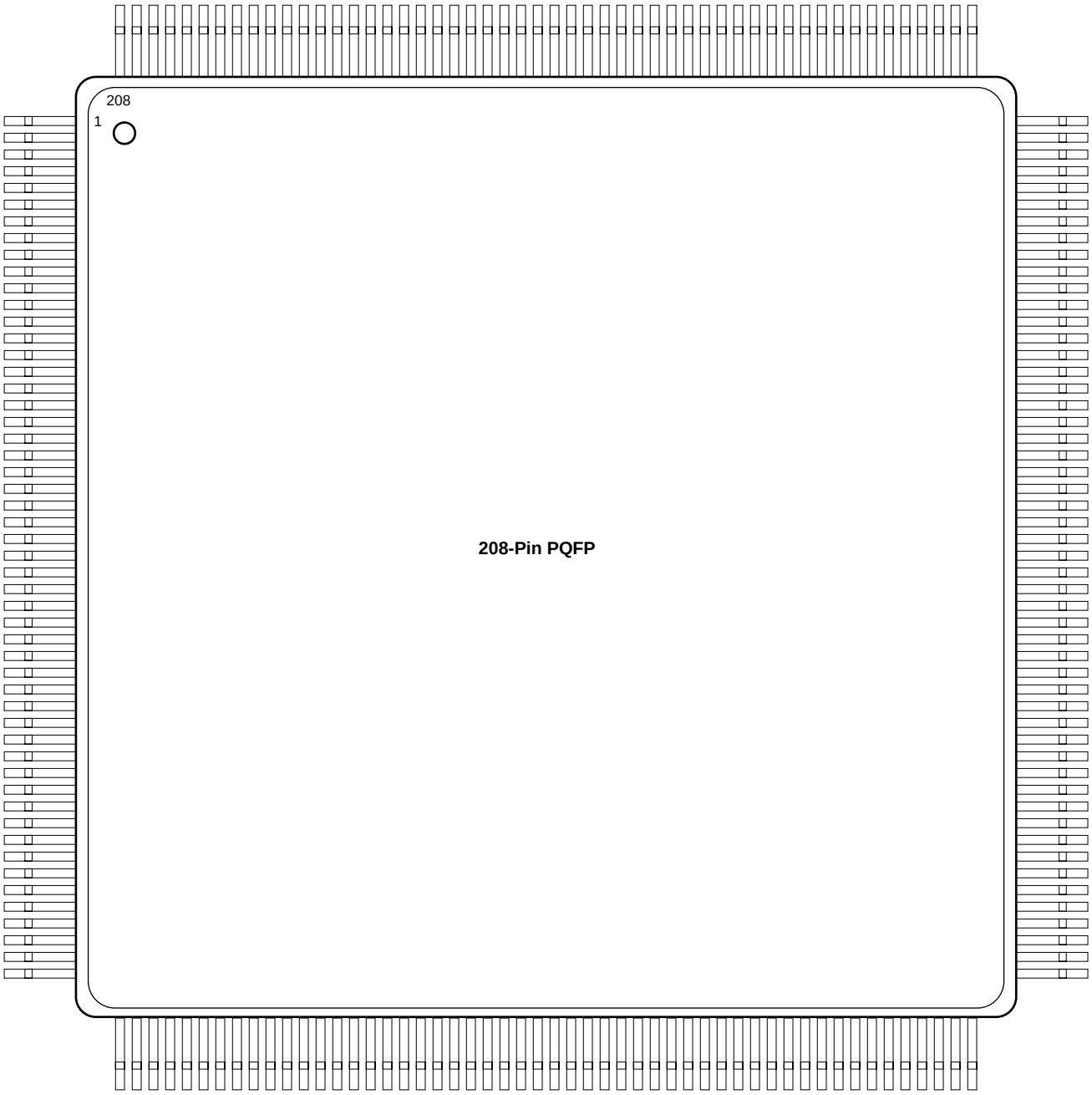
A54SX72A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.6		1.9		2.1		2.5	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.4		1.6		1.8		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t_{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.8		3.2		3.6		4.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.9		3.4		3.8		4.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.4		3.9		4.4		5.2	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.5		4.0		4.5		5.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.6		5.3		6.0		7.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.6		5.3		6.0		7.1	ns
t_{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0	ns

Package Pin Assignments

208-Pin PQFP (Top View)



208-Pin PQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	NC	NC	NC
26	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
107	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND
80	NC	NC	NC
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O
158	I/O	I/O	I/O

** Please note that Pin 65 in the A54SX32A—PQ208 is a no connect (NC).*

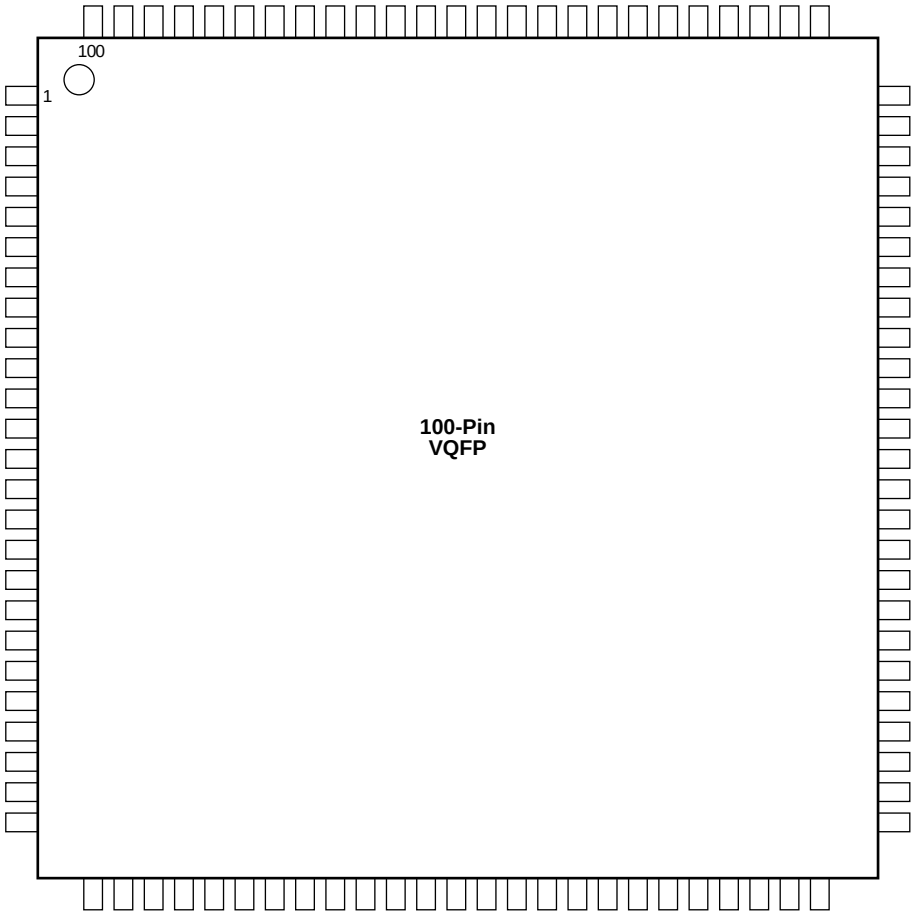
208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
108	NC	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND
132	NC	NC	NC
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O
145	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB
182	NC	NC	NC
183	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

** Please note that Pin 65 in the A54SX32A—PQ208 is a no connect (NC).*

Package Pin Assignments (continued)

100-Pin TQFP (Top View)



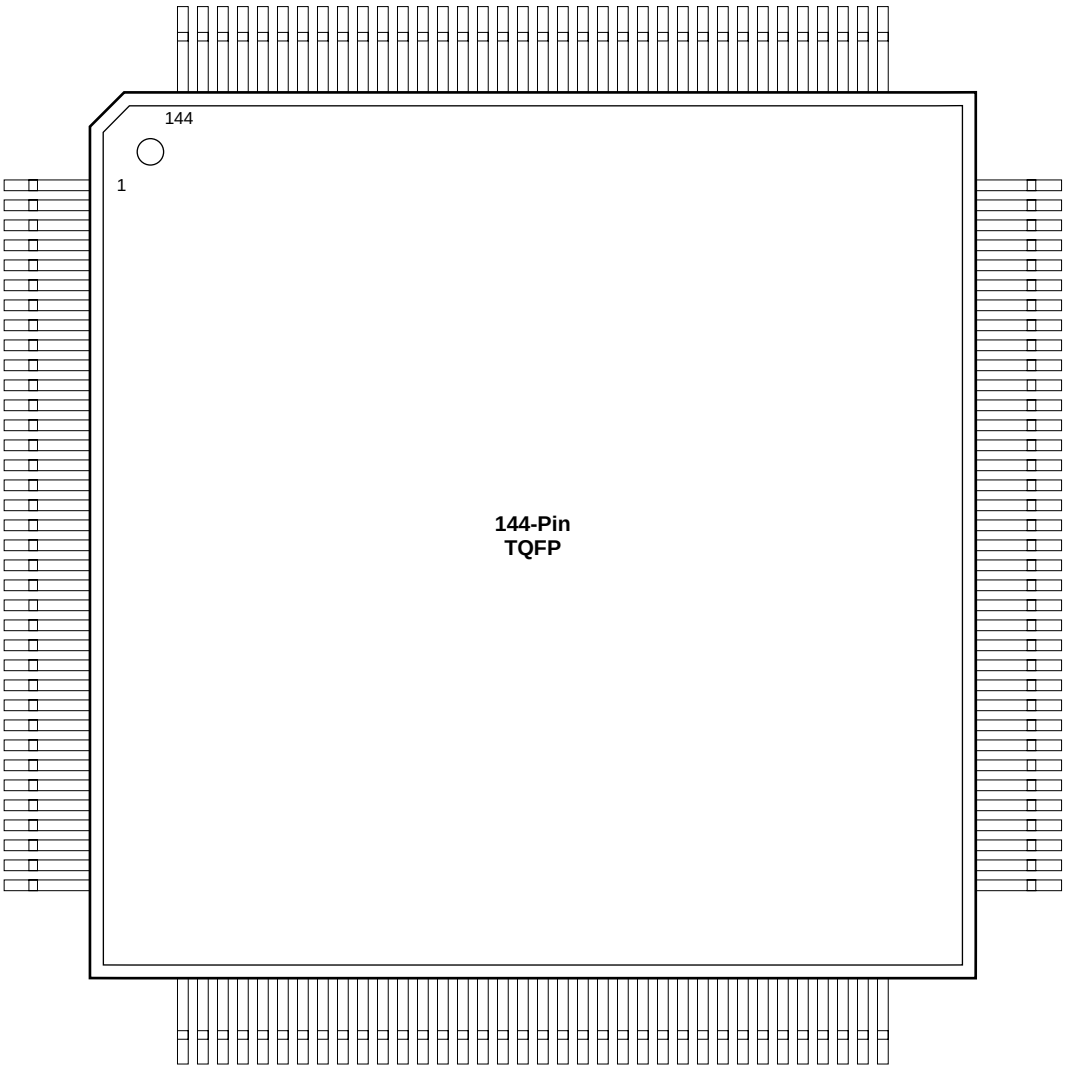
100-TQFP

Pin Number	A54SX08A Function	A54SX16A Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V_{CCI}	V_{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V_{CCI}	V_{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}
36	GND	GND
37	NC	NC
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V_{CCI}	V_{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V_{CCA}	V_{CCA}
68	GND	GND
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V_{CCI}	V_{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	NC	NC
90	V_{CCA}	V_{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

144-Pin TQFP (Top View)



144-Pin TQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}

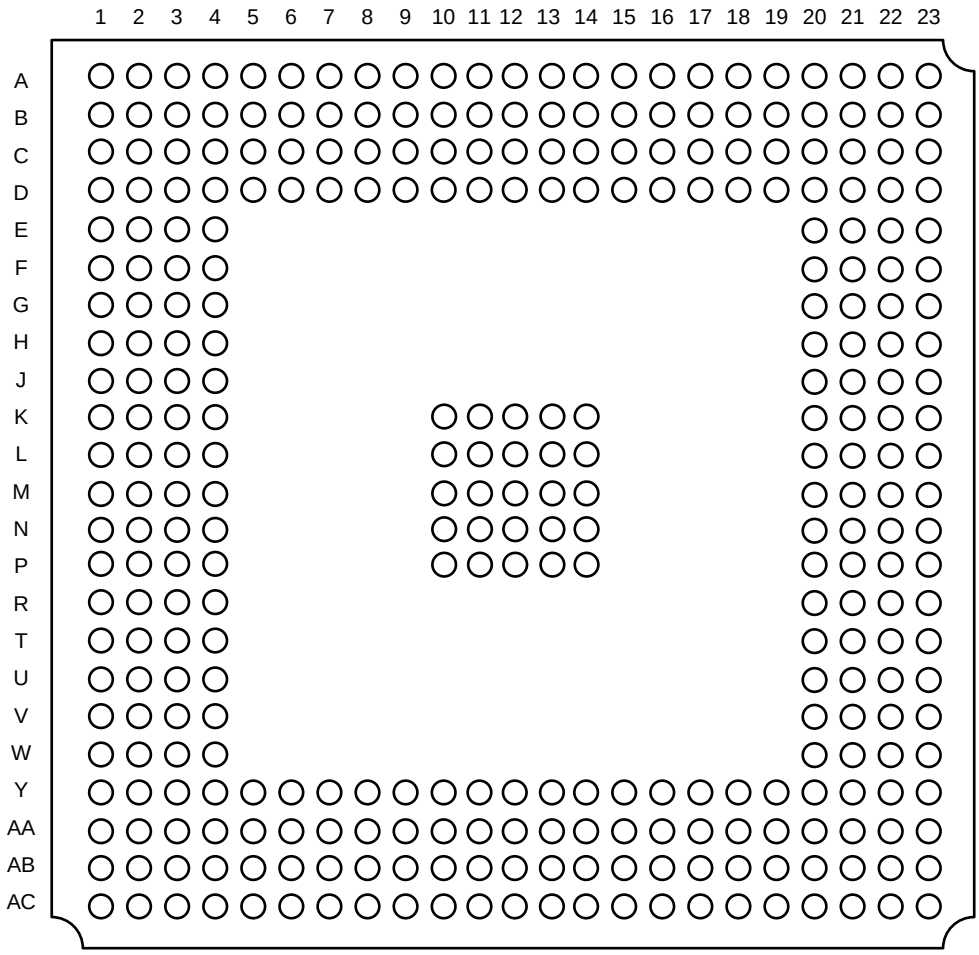
144-Pin TQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

329-Pin BGA (Top View)



329-Pin BGA

Pin Number	A54SX32A Function
A1	GND
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A2	GND
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
AA1	V_{CCI}
AA10	I/O
AA11	I/O
AA12	I/O
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA2	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O
AA23	V_{CCI}
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O

Pin Number	A54SX32A Function
AA9	I/O
AB1	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB2	GND
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AC1	GND
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC2	V_{CCI}
AC20	I/O
AC21	NC
AC22	V_{CCI}
AC23	GND
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O

Pin Number	A54SX32A Function
AC8	I/O
AC9	V_{CCI}
B1	V_{CCI}
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B2	GND
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
C1	NC
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C2	TDI, I/O
C20	I/O
C21	V_{CCI}
C22	GND
C23	NC
C3	GND
C4	I/O
C5	I/O
C6	I/O

Pin Number	A54SX32A Function
C7	I/O
C8	I/O
C9	I/O
D1	I/O
D10	I/O
D11	V_{CCA}
D12	NC
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D2	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
E1	V_{CCI}
E2	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
E3	I/O
E4	I/O
F1	I/O
F2	TMS
F20	I/O
F21	I/O
F22	I/O
F23	I/O
F3	I/O
F4	I/O
G1	I/O
G2	I/O
G20	I/O

329-Pin BGA

Pin Number	A54SX32A Function
G21	I/O
G22	I/O
G23	GND
G3	I/O
G4	I/O
H1	I/O
H2	I/O
H20	V_{CCA}
H21	I/O
H22	I/O
H23	I/O
H3	I/O
H4	I/O
J1	NC
J2	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
J3	I/O
J4	I/O
K1	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K2	I/O
K20	I/O
K21	I/O
K22	I/O
K23	I/O
K3	I/O
K4	I/O
L1	I/O
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L2	I/O
L20	NC
L21	I/O
L22	I/O
L23	NC

Pin Number	A54SX32A Function
L3	I/O
L4	NC
M1	I/O
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M2	I/O
M20	V_{CCA}
M21	I/O
M22	I/O
M23	V_{CCI}
M3	I/O
M4	V_{CCA}
N1	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N2	I/O
N20	NC
N21	I/O
N22	I/O
N23	I/O
N3	I/O
N4	I/O
P1	I/O
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P2	I/O
P20	I/O
P21	I/O
P22	I/O
P23	I/O
P3	I/O
P4	I/O
R1	I/O
R2	I/O
R20	I/O
R21	I/O

Pin Number	A54SX32A Function
R22	I/O
R23	I/O
R3	I/O
R4	I/O
T1	I/O
T2	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
T3	I/O
T4	I/O
U1	I/O
U2	I/O
U20	I/O
U21	V_{CCA}
U22	I/O
U23	I/O
U3	V_{CCA}
U4	I/O
V1	V_{CCI}
V2	I/O
V20	I/O
V21	I/O
V22	I/O
V23	I/O
V3	I/O
V4	I/O
W1	I/O
W2	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
W3	I/O
W4	I/O
Y1	NC
Y10	I/O
Y11	I/O
Y12	V_{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O

Pin Number	A54SX32A Function
Y18	I/O
Y19	I/O
Y2	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O